REMARKS

Applicants respectfully request reconsideration. Claims 1-25 were previously pending in this application. By this amendment, Applicants are canceling claim 2 without prejudice or disclaimer. Claims 1, 10, 12, 13, 14, 15, 16, 19, 23, 24 and 25 have been amended. No new claims have been added. As a result, claims 1 and 3-25 are pending for examination with claims 1, 10 and 19 being independent claims. No new matter has been added.

Rejections under 35 U.S.C. §112

The Examiner rejected claim(s) 10-18 and 25 under 35 U.S.C. §112.

The Examiner has rejected claim 10 for reciting "the core circuitry." That term appears as part of a description of circuitry that interfaces to external devices. Such circuitry is described elsewhere in the claim as "circuitry that interfaces to devices external to the data processing chip." This same terminology has been used in place of the phrase "core circuitry" and should resolve any issue with the claim language. Similar changes were made in claims 12, 13, 14, 15, 16 and 19 for consistency. These changes do not alter the scope of the claims and therefore do not add new matter.

The Examiner has also rejected claim 25 because it recites "the first value" without antecedent basis. Claim 25 depends indirectly from claim 19. "A first value" is recited in element a) of claim 19. The phrase "the first value" in claim 25 therefore has adequate antecedent basis.

Accordingly, withdrawal of the rejection of claim(s) 10-18 and 25 under 35 U.S.C. §112 is respectfully requested.

Rejection under 35 U.S.C. §102 based on Sullam et al.

The Examiner rejected claims 1, 2, 3 and 10, based on Sullam et al.

Claim 1 recites a device comprising internal circuitry clocked by a first clock signal and at least one interface circuit clocked by a second clock signal. A first programmable frequency

scaling circuit provides the first clock signal. A second programmable frequency scaling circuit supplies the second clock signal.

Sullam does not disclose such a device. The differences may be seen from an examination of FIGS. 1 and 2 of Sullam. FIG. 1 pictures a device including clocking circuitry that is shown in more detail in FIG. 2. Though FIG. 2 shows multiple programmable dividers, FIG. 1 makes clear that the outputs of those dividers is not connected such that internal circuitry is clocked by a first clock signal and an interface circuit is clocked by a second clock signal. FIG. 1 shows no connection between clocking circuitry 112 and input/output 108, which is understood to be the only interface to external circuitry disclosed in the reference. Accordingly, Sullam does not disclose a device with circuitry clocked as recited in claim 1.

Further, the reference does not recognize the advantages of separate control over the clock frequency of internal circuitry and an interface circuit as is recited in the claims. Accordingly, the reference does not suggest the claimed combination. Without such a disclosure or teaching of the claimed features, the claim is neither anticipated nor obvious in light of the reference and the claim should be allowed.

Claim 3 depends from claim 1 and likewise should be allowed.

Claim 10 expressly recites "clocking circuitry within the first circuitry using the first clock and clocking circuitry that interfaces to devices external to the data processing chip with the second clock." As described above, Sullam does not teach separate clock frequencies for internal circuitry and interface circuitry. Accordingly, the rejection of claim 10 should also be withdrawn.

Rejection under 35 U.S.C. §102 based on Shimoda et al.

The Examiner has rejected claims 1, 2, 3, 8 and 10 based on Shimoda et al. The Examiner points to FIG. 3 as showing programmable frequency scaling circuits 244 and 254. However, Applicants disagree that the reference describes circuits 244 and 254 as programmable. The structure of circuits 244 and 254 is not described in the reference and there is no indication that the function of those circuits is programmed as part of a method of operating the device. Rather, the reference describes that it is preferable that the "internal-to-peripheral clock frequency ratio is N:1 or N:2." Further, the reference describes that the "wiring area for

the clocks can be reduced." With no disclosure of programmable frequency scaling circuitry and references to constrained ratios and "wiring," it is a matter of speculation that circuits 244 and 254 are programmable and the reference cannot be read to fairly describe or teach programmable elements as claimed. Accordingly, the claim does not describe or suggest all the elements of claim 1, including a first programmable frequency scaling circuit that generates a first clock for internal circuitry and second programmable frequency scaling circuit that generates a second clock for an interface circuit that interfaces to external circuitry.

The dependent claims provide further distinguishing limitations. For example, claim 3 recites programmable dividers. Because the reference does not disclose any structure for elements 244 and 254, the reference cannot be fairly said to teach programmable dividers as claimed.

As to claim 10, the reference does not teach each element of the claimed method. For example, there is no teaching of the act b) of specifying a first frequency ratio or the act d) of specifying a second frequency ratio as part of a method of operating a data processing chip.

Rejection under 35 U.S.C. §103 based on Sullam et al. in view of Petersson et al

The Examiner has rejected claims 4-7, 9, 12-13, 16-20 and 22-24 based on Sullam et al. in view of Petersson et al. This rejection should be withdrawn for several reasons. First, the references are not properly combinable. Petersson et al. does not relate to design of devices that include internal circuitry and interface circuitry. Rather, it relates to a broad band frequency synthesizer and is therefore nonanalogous art. Second, even if combined, the references do not show all elements of the claim. Sullam et al. fails to meet the limitations of the independent claims as discussed above, and Petersson et al. does not supply a teaching or suggestion of the missing elements. Petersson et al. describes a broad band frequency synthesizer, but does not describe a device with internal circuitry and circuitry that interfaces to external circuitry clocked with separate programmable clocks.

Further, the Examiner asserts that the Petersson reference discloses loading of a programmed divider value when the control logic detects an end of a period of the first clock. Applicants respectfully disagree that the disclosure teaches loading a programmable divider as claimed. Petersson does not disclose a first clock and a second clock as recited in the claims.

The passage cited by the Examiner refers to using the output of the phase detector to control loading of a program value. In the present application, the phase detector 218 (see FIG. 3) does not control loading of a frequency divider and does not serve the same function as the first clock and does not meet the limitations of the first clock as recited in the claim. Therefore, the teaching in the reference relating to the output of the phase detector does not describe the claimed feature such as appears in claim 6, which does not recite an output of the phase detector but instead recites loading a programmed divider value when the control logic detects an end of a period of the first clock.

As regards claim 9, Applicants disagree that the reference teaches a control register as claimed.

As regards claim 12, the Examiner contends that the circuitry of the reference provides the ability to change frequencies and therefore perform the recited step. Circuitry that had the ability to perform the claimed method does not make the claimed method obvious if the circuitry was not operated according to the claimed method and there was no teaching or suggestion to operate the circuitry in that way.

Further, even if circuitry that could have been used in the claimed method were adequate to make a *prima facie* rejection, the references would still not render the claims obvious. The references do not describe operating a data processing chip meeting all of the limitations of claim 12 (including the limitations of claim 10 from which claim 12 depends). For example, the reference does not disclose operating a data processing chip to place it in a first power saving mode by changing the frequency ratio to derive a first clock while clocking circuitry that interfaces to devices external to the data processing chip with a second clock.

As regards claim 13, there is no teaching in the references of operating a data processing chip in a second power saving mode by reducing the frequency of the reference clock. None of the references relates to operating in one power saving mode and so do not teach or suggest two modes.

Claim 16 recites in further detail the advantages of the inventive architecture for a data processing chip. Claim 16 recites that the data processing chip may be placed in a power saving mode by changing the first frequency ratio that is used to drive a first clock to clock circuitry within the data processing chip without changing the frequency of the reference clock or the

second clock. As described in the application, the claimed chip architecture and claimed method of operation provide substantial flexibility in managing the power consumed by a data processing chip. Power saving mode can be exited quickly, allowing that mode to be entered for short periods. None of the references recognizes these advantages and therefore the references alone or in combination do not teach all elements of the claim.

As regards claim 19, the Petersson reference teaches using the output of a phase detector for controlling loading of a programmable frequency divider. It does not teach the approach recited in the claim. For example, it does not teach or suggest element d) "waiting until a defined time relative to the period of the second clock while holding the state of the first clock." Because none of the references teach this limitation, the claim is not obvious.

As regards claims 22-24, the Examiner has indicated these claims are rejected at paragraphs 9 and 10 but has indicated they would be allowable at paragraph 11. Regardless, these claims should be allowed. Claim 22 recites setting a value in a control register and claim 23, which further depends from claim 22, recites loading a programmable counter. In embodiments described in the present application, a separate control register and programmable counter provide greater flexibility in controlling a data processing chip, such as to actively manage the power of the device as it operates. Because these functions are not described or suggested in the reference, the references cannot be said to teach the limitations of these claims.

Rejection under 35 U.S.C. §103 based on Shimoda et al. in view of Petersson et al.

As described above, Shimoda et al. does not teach programmability as recited in the claims. Though Petersson et al. describes changing the frequency of a synthesizer, it does not teach or suggest separate programmability of clocks in a data processing chip as is recited in the claims. Accordingly, these references are not properly combinable because Petersson is nonanalogous art. Further, even if combined, the references would not result in the claimed structure or method. The combination of the references would lack at least the elements of the claims highlighted above. Furthermore, because Shimoda does not teach a programmable first clock and a programmable second clock, there is no motivation to apply the teachings of Petersson to the circuit of Shimoda.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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